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Attorney Docket No. MTI-31267 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Number:		6,762,125 B1
Issued	:	July 13, 2004
Patentee	:	William A. Polinsky et al.
Title	:	Modified Facet Etch to Prevent Blown Gate Oxide and Increase Etch Chamber Life

Certificate

CERTIFICATION UNDER 37 CFR 1.8(a) and 1.10 AUG 0 2 2004

I hereby certify that, on the date shown below, this correspondence is being:

of Correction

Mailing

■ deposited with the U.S. Postal Service in an envelope addressed to the Commissioner for Patents, Certificate of Correction Branch, P.O. Box 1450, Alexandria, VA 22313-1450.

37 CFR 1.8(a) **37 CFR 1.10**

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Date: 7-26-4 Patricia Peckham

Commissioner for Patents
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ATTENTION: Certificate of Correction Branch

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT
FOR PTO MISTAKE (37 C.F.R. SECTION 1.322(A))

Sir:

It is requested that a Certificate of Correction be issued correcting printing errors appearing in the above-identified United States Patent.

Attached is Form PTO-1050, with the text of the Certificate in the suggested form suitable for printing.

The column and line number where the errors occur in the issued patent are as follows:

Column 2, line 56: Replace "suicides" with --silicides--.

Column 3, line 12: Replace "comers" with --corners--.

Column 3, line 14: Replace "comers" with --corners--.

Column 4, line 29: Add --claims appropriately-- after "appended".

3 AUG 2004

REMARKS

The errors sought to be corrected in the specification are Patent Office printing errors.

Supporting documentation includes a copy of the relevant pages of the original specification filed on May 14, 2001, showing the original text of the specification to which changes were not made during the prosecution of the application to which correction is requested.

The requested corrections are to correct printing errors in the claims to conform with the specification and claims as allowed by the Examiner during prosecution. Issuance of a Certificate of Correction would not change either the scope or the meaning of the specification, and re-examination is not required.

As the errors listed are due to the Patent Office's printing mistakes, no fee is necessary in connection with this Certificate.

The Examiner is requested to contact the undersigned Attorney for Applicant should any questions arise with respect to this Request.

Please send the Certificate of Correction to:

Alan E. Wagner
Whyte Hirschboeck Dudek S.C.
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Dated: July 26, 2004

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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,762,125

DATED : July 13, 2004

INVENTOR(S) : William A. Polinsky et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 2, line 56: Replace "suicides" with --silicides--.
Column 3, line 12: Replace "comers" with --corners--.
Column 3, line 14: Replace "comers" with --corners--.
Column 4, line 29: Add --claims appropriately-- after "appended".

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PATENT NO. 6.762,125

No. of additional copies

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3 AUG 200

silver, nitrides thereof and silicides thereof.

The substrate 10 includes any semiconductor-based structure having a silicon base. The base of substrate 10 is to be understood as including silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. Furthermore, previous process steps may have been used to form regions or junctions in the base semiconductor structure or foundation. Typically, the substrate 10 will comprise at least one layer of material deposited on top of the silicon base. In one preferred embodiment, the uppermost layer of material of substrate 10, which contacts conductive structures 12, will be a dielectric material such as silicon dioxide or boron phosphosilicate glass (BPSG).

A first layer 16 is formed over the substrate 10 and conductive structures 12 as shown in FIG. 2. First layer 16 comprises a dielectric material 17, preferably silicon dioxide or BPSG. First layer 16 may be conveniently formed by chemical vapor deposition or any other suitable means.

As shown in Figure 3, the spaces 14 between the conductive structures 12 are not completely or uniformly filled during the formation of first layer 16. In particular, the bottom 37 and lower corners 36 of space 14 are covered with a thinner depth of dielectric material 17 than are the sidewalls 38 and upper corners 35. This nonuniform coverage of dielectric material 17 leads to the formation of undesirable voids, known as keyholes within the first layer 10 or between the first layer 10 and subsequent layers.

A facet etch is performed to provide a lower aspect opening for subsequent layers as shown in FIG. 4. The facet etch is conveniently performed by placing the semiconductor device 1 in a high vacuum reactor on a cathode for which a power source creates a radio frequency (RF) of 13.56 Mhz, while controlling the introduction of the etchant gases.

claims appropriately interpreted in accordance with the doctrine of equivalents.